A 2.4 GHz CMOS Transceiver for Bluetooth

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ABSTRACT — **A fully integrated CMOS transceiver tuned to 2.4 GHz consumes 46 mA in receive-mode and 47 mA in transmit-mode from a 2.7 V supply. The receiver achieves a sensitivity of –80 dBm at 0.1% BER, and an IIP3 of –7 dBm. The transmitter delivers a GFSK modulated spectrum at an output power of 5 dBm.**

I. INTRODUCTION

Bluetooth is a communication protocol enabling low-cost, short-range radio links between mobile phones, mobile PCs, and other portable devices. The Bluetooth standard specifies a 2.4 GHz frequency-hopped, spread-spectrum system that enables users to easily connect to a wide range of computing and telecommunication devices without the need for wires. It supports a data rate of 1 Mb/s with a Gaussian-FSK (GFSK) modulation scheme [1]. This paper describes a low-cost, low-power, and highly integrated solution for 2.4 GHz short-range radio applications, such as Bluetooth.

II. TRANSCEIVER ARCHITECTURE

Figure 1 shows the block diagram of the integrated CMOS transceiver. The transmitter uses a direct-conversion architecture to achieve low power consumption and high level of integration [2]. A quadrature oscillator takes the digital data and generates a continuous-phase binary FSK signal at base-band, followed by I and Q Gaussian low-pass filters to shape the spectrum. In contrast to conventional modulators, this approach eliminates the need for a DAC, and leads to a lower power dissipation. Single side-band Gilbert-type mixers up-convert the base-band GFSK spectrum directly to 2.4 GHz. A Class AB power amplifier consisting of a pre-amplifier and a driver stage boosts this signal and delivers a power of 5 dBm to a 50 Ω load, using an on-chip matching circuit. The measured s_{22} at the transmitter output is better than –12 dB across the 2.4 GHz band.

A clock generator is exploited to produce a clock frequency which coincides with the RF signal at the transmitter output, as required in a direct-conversion transmitter, yet positioning the VCO frequency far from that of PA. Shown in Figure 2, it consists of a divide-by-two which generates quadrature outputs at 800 MHz from the 1.6 GHz VCO, and two mixers that produce I and Q clocks at 2.4 GHz. Buffers are used between the stages to provide isolation, signal amplification, and filtering. Since the VCO frequency is 2/3rd of the PA output frequency, the radio is insensitive to direct or harmonic pulling issues. Measurements show that the VCO frequency remains undisturbed at an output power of up to +20 dBm, using an external power amplifier. As the synthesizer operates at 1.6 GHz, for 1 MHz channel spacing, the reference frequency is 2/3 MHz, obtained by dividing the 12 MHz crystal frequency by 18. The corresponding loop bandwidth is about 60 kHz, realized by on-chip resistors and capacitors.

Due to the mixing action, spurious signals accompany the 2.4 GHz desired signal. All the spurs are however, at least 1.6 GHz away from the clock, and are rejected by on-chip LC filtering at the clock generator mixer and its buffer. The on-chip inductors have a quality factor of about 5.5 at 2.4 GHz. These spurs are further attenuated by the on-chip filters at the output of the up-conversion mixers and PA.

The receiver uses a low-IF architecture with an intermediate frequency of 2 MHz to integrate the channel-select filter. Since the GFSK spectrum has energy at or near zero IF, 1/f noise and DC offset may significantly degrade the receiver performance. The 2 MHz IF positions the signal beyond flicker noise corner. DC offset is removed by using ac-coupling between amplifier stages without distorting the desired signal located at 2 MHz. The 3-dB bandwidth of the ac-coupling circuits is about 700 kHz.

As mixers are inherently noisy and nonlinear devices, the advantage of the above architecture to a dual-conversion transceiver is that one step of frequency conversion is done inside the clock generator, where noise or linearity is not an issue. This leads to lower power consumption, since only one down-conversion in the receive path is needed.

The receiver uses an inductively degenerated common-source amplifier [3] tuned to 2.4 GHz as the LNA (Figure 3(a)). At 2 MHz IF, the image will be inside the 80 MHz ISM band, that is, four channels away from the desired signal. Thus, the image reject requirements are relaxed and achieved by I and Q mixers, and an on-chip complex-domain band-pass filter [4] centered at 2 MHz. All the filters inside the transceiver chip, including ac-coupling stages and the synthesizer on-chip loop filter, use an

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internal calibration circuit to adjust their frequency characteristics over temperature and process variation (Figure 1).

After the channel selection, the desired signal is amplified by a limiter to a well-defined level regardless of the input signal power, and the received signal strength is indicated. The Limiter consists of a buffer, followed by three stages of amplifiers, each with 8 dB gain, as shown in Figure 3(b). The outputs of the 8-dB gain amplifiers, as well as the output of an 8-dB loss stage outside the signal path are fed into digital rectifiers. Each rectifier generates 2 bits, leading to 40 dB dynamic range at 4 dB steps. These 10 bits are converted to a 4-bit Grey code by a logic unit, and passed to the base-band chip through a 4-wire interface for transmitter output power control. The signal is then limited by a 25-dB gain stage. An analog discriminator, consisting of I and Q differentiators and multipliers, demodulates the down-converted signal. A slicer converts the analog output to digital bits by adjusting the DC level of the analog output, using peak and valley detectors. Thus, any DC offset at the demodulator output, produced due to frequency errors, is removed by the slicer. The receiver can handle frequency errors of up to ±150 kHz.

III. EXPERIMENTAL RESULTS

The transceiver IC is fabricated in TSMC 0.35 µm CMOS process. It includes all the receive and transmit functions, such as VCO, synthesizer, modulator, demodulator, and PA. Except one capacitor for the LNA input matching to 50 Ω, a 12 MHz Crystal, and a few resistors to set the bias currents, no external components or filters are needed. All the I/O and supply pads, including RF pads, use ESD protection.

The receiver active current is about 46 mA, whereas the transmitter drains 47 mA, of which 15 mA is consumed by the VCO and synthesizer, and 12 mA by the clock generator. In power-down mode, the transceiver current reduces to less than 50 µA. All the biases are generated internally by band-gap circuits. Figure 4 shows the receiver BER versus the input signal power, measured by applying a 1 Mb/s, GFSK-modulated input at 2.44 GHz. At a BER of 0.1% as specified in Bluetooth, the minimum detectable signal is about –80 dBm, 10 dB better than the required sensitivity. To characterize the stand-alone demodulator, a large additive white Gaussian noise (AWGN) is superimposed on the desired GFSK signal to bypass the internal noise of the receiver. Thus, the demodulator input SNR will be equal to the one measured at the receiver input. For 0.1% BER, it requires about 18 dB of signal-to-noise, very close to the theoretical value. The receiver deduced noise figure is about 15 dB.

The transmitter output spectrum when pseudo-random data applied to its input is shown in Figure 5(a). The output power at 2.44 GHz is about 5 dBm at nominal temperature, and drops by only 2 dB at 85° C. Figure 5(b) shows the transmitter eye diagram when demodulated by an ideal receiver. The modulation index is about 160 kHz, and has less than ±3% variation over the temperature range of –25° C to 85° C, and among different IC samples. The zero-crossing error is about ±1/10 of a symbol period, well bellow the Bluetooth requirement of ±1/8.

Figure 6(a) shows the receiver in-band blocker rejection. The co-channel rejection is set by the demodulator capture range, whereas the interferers at ±1 MHz, and ±2 MHz away are rejected by the channel-select filter roll-off. The filter attenuation at 1 MHz and 2 MHz away are respectively 18 dB and 50 dB. The image blocker located at +4 MHz away is rejected by 25 dB, corresponding to an image rejection of about 43 dB. Figure 6(b) shows the two-tone strength versus the desired signal power at 0.1% BER. At an input of –64 dBm, the two-tone power is –32 dBm, corresponding to an IIP3 of about –7 dBm, 10 dB better than required IIP3 specified in Bluetooth standard.

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